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CARBON NANO TUBE FIELD EFFECT TRANSISTOR:A REVIEW

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ABSTRACT

Carbon Nano Tube Field Effect Transistor (CNTFET) has various extraordinary electrical and mechanical properties and due to this CNTFET is turning out to be the forefront material for future electronics. In this paper, the review of CNTFETs is presented. MOSFET technology has limited scope for further enhancement. With a motivation to find alternatives, we explore the domain of CNTFETs. The structure, operation and the various performance parameters have been discussed. The effect of threshold voltage, temperature, channel length,delay and power consumption for both CNTFETs and MOSFET devices have been discussed. Previous studies show that CNTFETs are far better than MOSFET device. It is propsed as an alternative to MOSFET because of its promising features. However, challenges faced by CNTFETs have been discussed.

KEYWORDS: CNTFETs, MOSFET, Chirality, Threshold voltage, Temperature, Channel length

INTRODUCTION

The future of electronic industry is focusing more on portability. Size and power dissipation are the two main parameters of prime concern for portable electronic devices.Inconventional planar CMOS scaling is expected to become increasingly difficult. The channel length of metal oxide silicon based field effect transistor (MOSFETs) is limited to 10nm range and further reduction in channel length result into direct source to drain tunneling. Due to direct tunneling, gate leakage current and sub threshold leakage current increases,this is in turn increases the idle power required by the device. To overcome these limitations, CNTFETs became an attractive alternative to the conventional MOSFETs. In comarision to MOSFETs, CNTFETs possesses a very high k gate dielectric, quasi-ballistic transport at low voltage, higher transconductance(almost four times), higher drive current, higher average carrier velocity(almost twice), lower heat dissipation and higher on off current ratios. Apart from all these advantages, there are various challenges related to CNTFETs that need to be addressed before replacing it with practical transistors. These challenges includes variation in the quality of CNTs, effect of chirality on tube diameter, difficulty in mass production and reliability issues due to varying environmental conditions.This paper introduces the carbonnano tubes, the structure and modeling aspects of CNTFET, deals with comparision of performance parameters of CNTFETSs and MOSFETs devices and finally discuss challenges in CNTFETS.

CARBON NANO TUBE (CNT)

CNT is discovered by Ijima in 1991. It is in cylindrical structure of graphene ofnano- scaled diameter rolled up to form a tube shown in fig. 1. Depending on how the roll –up of graphite sheet occurs during the growth process, carbon nano tubes can exhibit semiconducting as well as metallic character. It can be classified as SWCNT(Single Walled Carbon Nano Tube) and MWCNT(Multi Walled Carbon Nano Tube) shown in fig. 2 where multi-layers of graphene are rolled as a concentric tube[1].

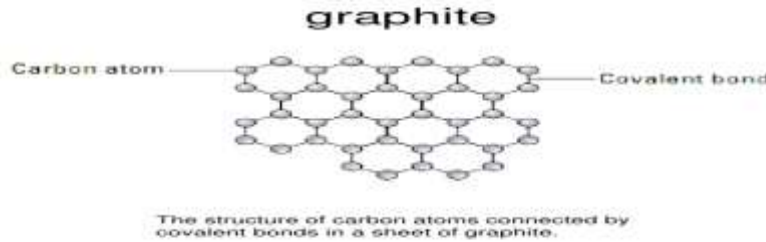

Figure 1: Structure of Carboon Nano Tube[1]

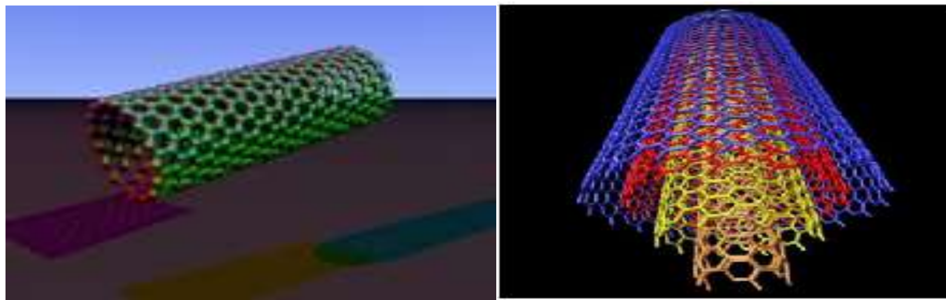

Figure 2: SWCNT and MWCNT [1]

Depending on chirality, SWCNTs can be metallic or semiconductor. Chirality of CNTs can be decided by two terms- Chiralvector C and chiral angle θ. Chiral vector C depends how the graphite sheet is rolled up to form cylinder and it is represented by pair of chiral indices(n,m) and it is given by:

$$C = na_1 + na_2 \qquad (1)$$

Where n and m are the integer of the unit vectors along the graphene structure associated with two unit vectors a_1 and a_2 respectively.While chiral angle θ is an angle at which graphene sheet is rolled up to form a carbon nano tube and it is given by:

$$\theta = \tan^{-1} \frac{\sqrt{3m}}{m+2n} \qquad (2)$$

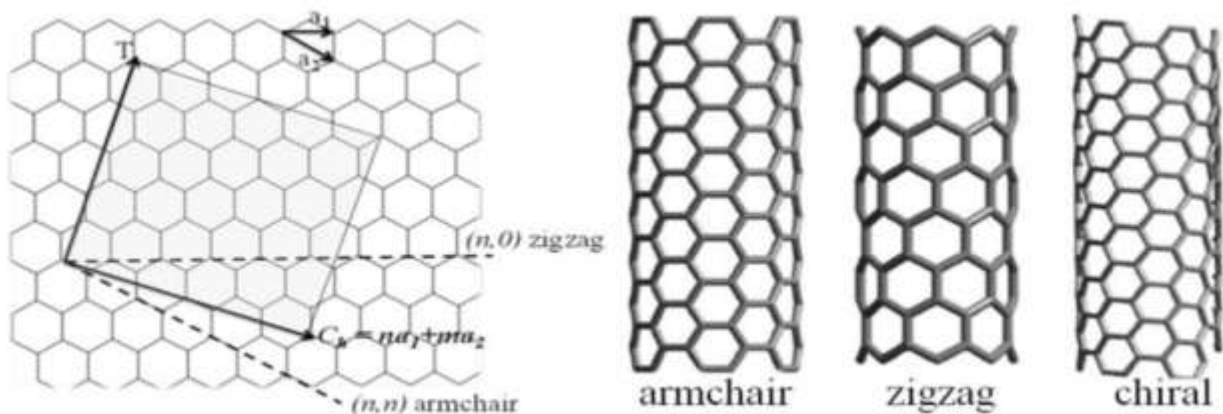

Figure 3: Geometry of CNT[2]

On the basis of C and θ, CNTs are classified into three types as shown in Fig 3:

(a) Zig-Zag (θ = 0, m = 0)
(b) Arm Chair (θ = 30º, n = m)
(c) Chiral(0<θ<30º , n ≠m)

If the value of n-m is dividible by 3 ,SWCNT behave as a metal otherwise it behaves as a semiconductor with small band energy gap varying from 0.1 to 2 eV.
The diameter of CNT also depends on its chirality and it is given by:

$$d = \frac{\sqrt{3}ac}{\pi}\left(\sqrt{n^2 + nm + m^2}\right) \quad (3)$$

Where d is the diameter of tube and a_c is the bond length of carbon atom, which is nearly equal to 1.44 Å for nano tubes.
For armchair tube

$$(n = m),\ d = \frac{3ac}{\pi}n \quad (4)$$

For zig-zag tube

$$(m = 0),\ d = \frac{\sqrt{3}ac}{\pi}n \quad (5)$$

In CNTFET, pure semiconducting SWCNT of specific dimension(depends on its chirality) is used as a conducting channel between source and drain in conventional silicon MOSFET. The operation of CNTFET is similar to MOSFET whereas in place of bulky silicon channel, thin CNT film channel carry electrons from source to drain terminal[3]

CARBON NANO TUBE FIELD EFFECT TRANSISTOR (CNTFET)

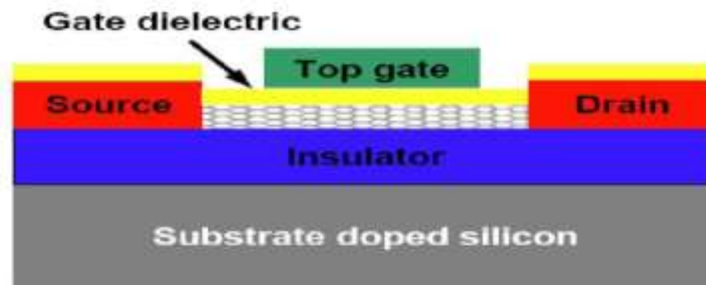

Figure4: Structure of CNTFET[4]

CNTFETs used carbon nano tubes in semiconductor form as channel instead of silicon in MOSFETs. The CNTFET is a four terminal device and operation of CNTFET is similar to a MOSFET. In fig.4 the main structure of transistor made of silicon. One or more carbon nano tubes are used as channel between source and drain. The drain and source are heavily doped to have access carriers near the conduction band which can easily conduct an application of voltage source. A SiO_2 substrate acts as the insulator between the metal contacts and the semiconductor part. A voltage is applied between the source and drain terminals and current is controlled by the voltage applied at the gate[4-5].

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COMPARISION OF CNTFET AND CMOS DEVICES

A Effect of chiral vector:

The threshold voltage of CNTFET is defined as gate to source voltage,which is required to turn ON and OFF the transistor. CNTFETS possess a unique property according to which its threshold voltage can be controlled by changing its chiral vector and diameter. The threshold voltageis given by:

$$V_{threshold} = aV_{\pi} / \sqrt{3} e\, d \qquad (6)$$

Where V_{π} is the bond energy of carbon atoms, a = 2.49 Å is the lattice constant and e is the electron's quality of the electricity. The threshold voltage of CNTFETs is higher when the difference of chiral vector (m,n) is small and vice versa [6-7].

Analysis: It is observed from twelve different chiral vector pairs starting from (4,0) to (26,12) and analyzed their corresponding threshold voltages. Higher threshold voltages can be achieved at a smaller value of m and at n= 0. Threshold voltage goes on decreasing while increasing in (m,n) shown in fig.5.

Table 1.Threshold voltage w.r.t. different Chiral vector[7]

Chiral Vector	(m-n)	Threshold Voltage
(4,0)	4	0.69
(6,2)	4	0.66
(16,12)	4	0.17
(8,0)	8	0.59
(9,1)	8	0.51
(17,9)	8	0.18
(11,0)	11	0.45
(13,2)	11	0.33
(24,13)	11	0.12
(14,0)	14	0.33
(17,3)	14	0.24
(26,12)	14	0.12

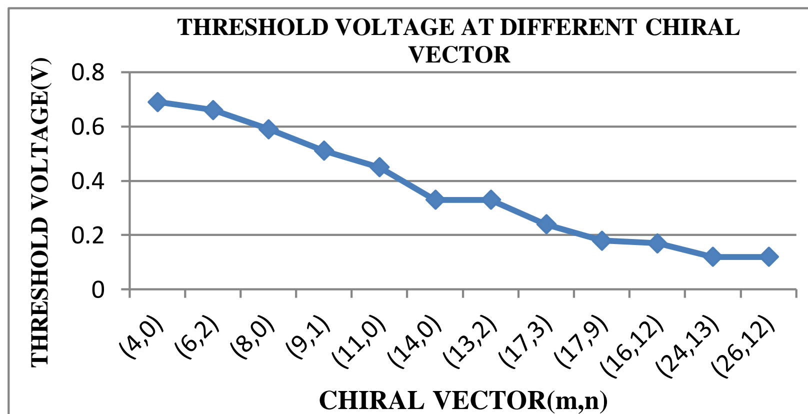

Figure 5: Threshold voltage decreases with increase in chiral vector(m,n).[7]

B Effect of Temprature:

The characteristics and circuit behavior of MOSFETs are changes with the increase of temperature. The maximum tolerable temperature of silicon device 150 degree. Because of strong covalent carbon-carbon bonding at sp^2 hybrdization, carbon nano tubes are inert chemically and are able to transport large amount of electric current.

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Carbon nano tubes are able to conduct heat nearly as diamond.

Table 2.Threshold voltage W.R.T. temperature.[7]

Temprature(ºC)	Threshold Voltag
27	0.210
47	0.210
67	0.210
87	0.210
107	0.202
127	0.198
147	0.194
167	0.191
187	0.187
207	0.180
227	0.164

In CNTFET devices effect of temperature on threshold voltage is negligibally small as shown in table 2. The analysis of negative temperature is also shown in table 3.

Table 3.Threshold voltage W. R .T. temperature.[7]

Temprature(ºC)	Threshold Voltag
-10	0.221
-20	0.229
-30	0.238
-40	0.243
-50	0.249
-60	0.256

Analysis :From the analysis it is shown that the affect of temperature hardly affects the threshold voltage in CNTFETs which is not possible in case of MOSFET as it operates at 150ºC and the characteristics of devices parameter changes at higher temperature. It is observed from table 2, that there is slightly deviation in threshold voltage at higher temperature. It is shown in table 3, that lower down the temperature in negative domain, 3.5% increment in threshold is observed, which negligibly affects the characteristics of CNTFET device. It is analyzed that the drain current vs. gate voltage at different drain voltages of CNTFET device and observed the threshold voltage is almost same in all temperature considered and there is small variation in threshold voltage whole increasing and decreasing the temperature, which is negligibly small[7-9].

C Effect of channel length

As we scaled down in nanometer regime of MOSFET in order to achieve higher packing density, the threshold voltage is also scaled, consequently the leakage power increases[10-13]. Leakage current has become the limiting factor for oxide thickness thinner than 1.5 nm. The current drive will increase as we decrease the channel length Much of the scaling is therefore driven by decrease in channel length. If only this parameter scaled many parameters are encountered, such as increased electric field. If the channel length becomes too short, the depletion region from the drain can reach the source side and reduces the barrier for electron injection. This is known as punch through, and because of this, devices characteristics degrades.

In long channel length devices, the gate is completely responsible for depleting the semiconductor. In short channel devices, part of depletion is accomplished by the drain and source bias. Since less gate voltage is required to transistor deplete, the barrier for electron injection from source to drain decreases. This is known as drain induced barrier lowering (DIBL). For both the devices CNTFET as well as MOSFET, channel length is taken from 100nm to 10nm for analysis.

Table 4. Threshold voltage w.r.t. different channel length[7]

Channel length effect of different devices		
Channel length (nm)	Threshold voltage(V)	
	CNTFET	**MOSFET**
100	0.227	0.241
90	0.227	0.241
80	0.227	0.241
70	0.228	0.242
60	0.228	0.242
50	0.229	0.243
40	0.231	0.245
30	0.239	0.247
20	0.263	0.248
10	**0.605**	**0.168**

Analysis : It is analysed from table 4, that in CNTFET as the channel length goes down from 20 nm to 10 nm the threshold voltage increases rapidly, whereas in the case of MOSFET devices threshold voltage decreases sharply which leads more leakage power and finally device degrades in term of performance while channel length reduces from 20nm to 10nm. The advantage of using CNTFET device in nanometer regime is to increased threshold voltage at 10 nm and beyond channel length. In case of MOSFET while reducing the channel length the threshold voltage is also reduced which lead to more leakage power[7].

D Effect of ballistic transport on Power consumption and Delay

Power cossumption and delay of CNTFET based gates is much lower than the CMOS counterparts because of the phenomena of ballistic transport. Ballistic transport is the transport of electrons in a medium having negligible electrical resistivity caused by scattering. Without scattering, electrons simply obey Newton's second law of motion at non-relativistic speeds.CNT shows ballistic conduction at room temperature. For SWCNT, it is 200nm scale. For MWCNT, both diffusive and ballistic properties are found. MOSFET does not show ballistic conduction because gate voltage holds some charge in the channel at the beginning[1,14].

From the study of basic gates such as inverter, nand and nor and the results for delay and power consumption have been tabulated in table 5. This is taken from CNTFET libraries provided by Nanoelectronics Lab at Standford University.

Table 5.Comparision between CMOS and CNTFET circuits in HSPICE[15]

Circuit	**FET**	**Delay (in ps)**	**Power (in uW)**
Inverter	CMOS	16.58	9.81
	CNT	3.78	0.25
2 Input NAND	CMOS	24.32	20.67
	CNT	5.98	0.69
2 Input NOR	CMOS	39.26	22.13
	CNT	6.49	0.48

Analysis :It is observed from this table 5, the power consumption and delay of CNTFET gates is much lower than the CMOS. This performance enhancement trend is a major motivation towards usage of CNTFET circuits to get better performance at lower power levels. However, the advantages observed above are assuming have error free basic gates. A lot of process variations have much adverse effects on CNTFETs which can significantly lower the performance[15].

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CHALLENGES WITH CNTFETs

The CNTFET technology faces several challenges due to unavoidable process variations that occur. These variations may not only degrade the performance but in extreme conditions may also lead to failure of CNTFET based logic circuits. It has been shown that CNTs are less sensitive to conventional CMOS process variations such as oxide thickness, channel length, doping concentration and channel width etc. and possess CNT variations. CNT process variations include CNT doping variations, variationsin CNT chirality, diameter, density and CNT alignment. Imperfections such as mispositioned CNTs and presence of metallic CNTs also effect performance parameters. These imperfections may cause increased gate delay, reduction in noise margin, excessive leakage current or incorrect functionality in logic circuits[15-16].

Following are the major CNT-specific variations:

1) **CNT density variation:**Chemical synthesis process used for the growth of CNTs does not provide precise control on the location of grown CNTs. This results in few CNTs being placed comparatively closer to others, which leads to variation in CNT density. As a result number of CNTs present in fixed width of CNTFET may vary affecting ths amount of current flowing.
2) **Metallic-CNT induced count variation:** CNTs display semiconducting or metallic properties; the presence of metallic CNTs result in conducting channel whose resistance cannot be controlled by Gate voltage. Metallic CNT physically manifest themselves as a short between drain and source. This results in excessive leakage current which causes undesirable effects of increasing power consumption and delay along with inferior noise performance and sometimes defective functionality too.
3) **CNT diameter variation:** Diameter variations occur due to chirality variation and depend significantly on the CNT growth process. Typical CNT diameters range from 0.5nm to 3nm. The band-gap of a CNTFET is determined by the CNT diameter and hence diameter variations can cause variation in CNT threshold voltage.
4) **CNT misalignment:** This refers to misalignment in the direction of CNTs. Along with mispositionedCNTs it results in a change in the effective CNT length in the CNTFETs channel. It may also result in short between CNTs in the CNTFETs and can cause incorrect logic functionality or reduction in drive current.
5) **CNT doping variation:** Variation in doping concentration in the source and drain regions; highly doped CNTs are required to exhibit unipolar behaviour.
6) **High background noise**.-Due to the inherent nature of carbon molecules the back ground noise goes higher which creates a trouble in operation of CNTFETs.
7) **Parasitic capacitance and huge external resistance**-many times it has been seen that CNTFETs channel CNTs grow inherent capacitance due to which we get deviation in the performance. Also due to the array of CNTs in the channel the resistance of channel increases and we have a very low charge mobility which reduces the precision of device.
8) **Life time**-The CNTs have a very small lifetime when exposed in oxygenous environment so this is a big trouble for longer working devices. Exposure to open air can cause an n-type CNT to revert back to p-type.

CONCLUSION

The review of CNTFETs are presented. This paper basically gives an introduction to CNT and CNTFETs.We analysed that the effect of variation in chiral vector on threshold. At low value of chial pair the threshold voltage is higher, whereas at high value of chiral vector the threshold voltage comes lower.It isanalysed that the effect of temperature on threshold voltage is very less or negligibly small and the channel length below 10nm, the threshold voltage in CNTFET is drastically increases while in MOSFET the threshold voltage is decreases. Finally we analysed that power cossumption and delay of CNTFET based gates is much lower than the CMOS counterparts because of the phenomena of ballistic transport. This paper showing that the CNTFETs appear to be similar to that of CMOS and simple MOSFETs in their characteristics and have a better performance but come with some mind boggling challenges have all potential to be the next generation basic devices for nano circuit fabrication.

REFERENCES

[1] Md. AlamgirKabir, "Performance analysis of CNTFET and MOSFET focusing channel length, carrier mobility and ballistic conduction in high speed switching", IJAMSE, Vol.3, No.3/4, October 2014.
[2] OlfaKanoun, "Flexible carbon nano tube films for hogher performance strain sensors", sensors 2014, 14(6), 10042-10071; doi:10.3390/s140610042.
[3] GauravSapare, " Simulation and Analysis of CNTFET based inverter", ARPN Journal of Engineering and Applied Sciences, Vol. 10, No. 12,July-2015.
[4] S.V.Srikanth, "Design of Logic Gates uing CNTFETs", ISSN:2394-3661, Vol.-2, Isue-4, April 2015

[5] Kaushik Roy, and Vivek De, "Carbon Nanotube Field-Effect Transistors for High-Performance Digital Circuits—Transient Analysis, Parasitic, and Scalability", IEEE Transactions On Electron Devices, Vol. 53, NO. 11, Nov-2006.
[6] R.Sahoo and R. R. Mishra, "simulations of Carbon nano tube field effect transistors, International Journal of Electronics Engineering Research, ISSN 0975-6450.
[7] Sanjeet Kumar Sinha and SaurabhChoudhary, "Comparative study of leakage power in CNTFET over MOSFET device", Journal of Semiconductors, Vol. 35, No. 11, Nov-2014.
[8] Wei B Q, Vajtai R, Ajayan P M." Reliability and current carryingcapacity of carbon nanotubes.",Appl PhysLett, 2001, 79(8): 1172
[9] Appenzeller J., " Carbon nanotubes for high-performance electronics:progress and prospect.", Proc IEEE, 2008, 96(12): 2011
[10] Terada K, Muta H., " A new method to determine effective MOSFETchannel length.", Jpn J ApplPhys, 1979, 18: 953
[11] Chern J G J, Chang P, Motta R F, et al., " A new method to determineMOSFET channel length.", IEEE Electron Device Lett, 1980,
[12] Taur Y, Mii Y J, Logan R, et al., " On effective channel length in0.1 _m MOS FET's.", IEEE Electron DeviceLett, 1995, 16: 136
[13] Jain S., " Measurement of threshold voltage and channel length ofsubmicron MOSFET's." , Proc Inst Elect Eng, 988, 135(1): 162
[14] J. Guo et al., "Assesssment of Silicon MOS and Carbon Nanotube FET Performance Limits using a General Theory of Ballistic Transistor", Electron Devices Meeting, 2002. IEDM '02 International, pp. 711-714
[15] Amitesh Narayan, SnehalMhatre, YamanSangar, "ProbablisticModelling of Performance Parameters of Canrbon Nanotube Transistors." ,IEEE paper template.
[16] SabyasachiTiwari, "CNTFETs the Next Generation of FETs." , Vol. 2, No. 4, IJEDR-2014.